A Quasi-Microstrip Traveling-Wave Power Divider/Combiner for Use in High-Density Packages

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***Abstract*— A low-loss miniature microstrip 4-way traveling-wave divider/combiner (TWD/C) that incorporates the package effects into the circuit design, i.e., the microstrip transmission line impedances partially includes the package wall as a ground plane, is presented. The TWD/C was designed using a full-wave electromagnetic simulator. Additionally, this TWD/C has less than a 0.3-dB insertion loss and a 1.6:1 VSWR at all ports over a 6-GHz bandwidth.**

I. Introduction

TRAVELING-wave power dividers/combiners (TWD/C's) have been used for combining 4 to 6 power amplifiers because they are compact, have low loss [1], [2], and are viable well into the millimeter-wave frequency range [3]. TWD/C's are designed using a cascade of Wilkinson power dividers, each having a different power division ratio. For example, a 4-way TWD/C uses the power division rations of 4:1, 3:1, and 2:1.

Since most systems require power amplifiers with a high power-added efficiency, the combiner must have low loss. This letter presents a low-loss compact design and fabrication technique that uses quasi-microstrip (microstrip transmission lines whose impedances depend partially on the package wall) and miniature resistors fabricated on GaAs to reduce the combiner's dimensions.

II. Design Theory

Fig. 1 shows a schematic of the TWD/C. Each of the transmission line sections has an electrical length of about 90 degrees. The schematic shows the Wilkinson dividers separated by two 90 degree sections. These sections were added to physically separate the outputs of the combiner because the final assembly had to accommodate relatively wide MMIC chips. Additionally, the transmission line impedances were constrained to be no greater than 77 ohms and no less than 20 ohms on a 0.38-mm thick alumina substrate ($\varepsilon_r = 9.9$) due to loss considerations and transverse resonances, respectively.

Generally in microstrip circuit designs, sufficient space between the circuit, the package walls, and the lid is provided in order to prevent any interactions. Since a very small size for our TWD/C was desired in the transverse direction, we treated the package as a part of the circuit design. In our design, the microstrip conductor is placed a quarter of a line width (two-thirds of a substrate thickness) from the wall. The side wall effect can be calculated either by using the analysis of the odd-mode propagation in a coupled microstrip lines [4] or using the modified microstrip models in commercial CAD tools. A full-wave type electromagnetic simulator, "em" by Sonnet Software was used to analyze the present divider/combiner due to its versatility in incorporating the effect of enclosure, continuously variable spacing between the microstrip conductor and the wall, and the interactions between the circuit components.

Table I contains two simple example analyses results which determined the relationship of the microstrip line's impedance

TABLE I
THE CHARACTERISTIC IMPEDANCE AND EFFECTIVE DIELECTRIC CONSTANT FOR TWO MICROSTRIP LINE WIDTHS AS A FUNCTION OF THE DISTANCE FROM THE PACKAGE WALL

Distance from Wall ($h = 0.38$ mm, substrate thickness), H	1.05-mm Line Width, W		0.38-mm Line Width, W	
	Z_o	ε_{eff}	Z_o	ε_{eff}
$10 \times h$	26.4	7.8	49.6	6.9
$3 \times h$	26.2	7.7	49.2	6.8
$2 \times h$	25.9	7.6	48.7	6.7
$1 \times h$	25.2	7.3	47.1	6.4
$0.5 \times h$	23.8	6.9	42.9	6.1
$0.33 \times h$	22.7	6.7	40.1	5.9

TABLE II
THE WIDTHS OF THE QUASI-MICROSTRIP USED IN THE TWC/D DESIGN VERSUS THE MICROSTRIP WIDTHS NECESSARY FOR AN UNPACKAGED TWC/D DESIGN

Design Impedances	Microstrip Width (μm)	Quasi-Microstrip Width (μm)
41.2	528	528*
27.7	1016	950
24.0	1250	1050
20.4	1574	1420
28.9	956	840
25.5	1150	1070
50.0	356	300

*This line is located far enough (>700 μm) from the package wall for its width to be unaffected.

Manuscript received January 27, 1993.

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IEEE Log Number 9208972.

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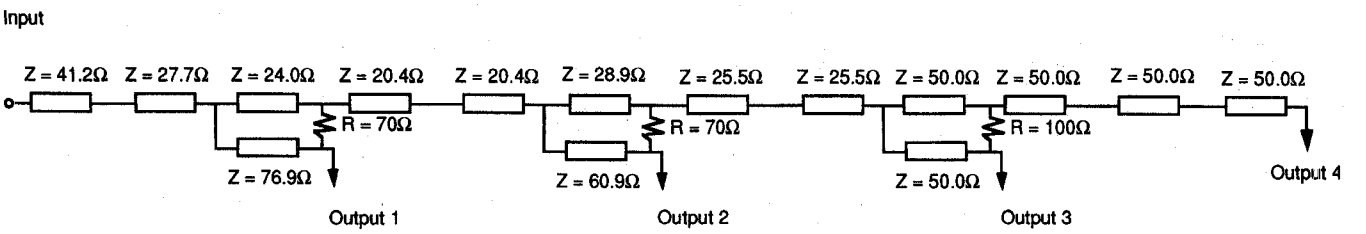

Fig. 1. Schematic of the traveling-wave combiner. All electrical lengths are 90°.

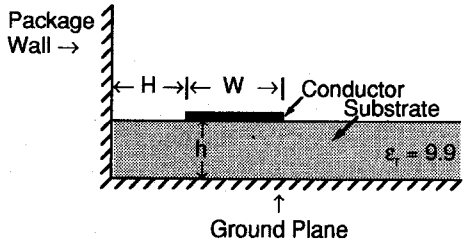

Fig. 2. A cross-sectional view that shows the relationship of the microstrip line to the package wall and the ground plane.

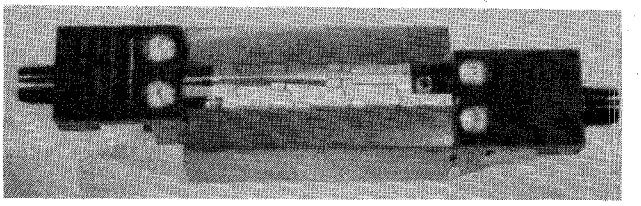

Fig. 3. Photogragh of a pair of TWD/C's in a back-to-back configuaration and mounted in a test fixture constructed to simulate the final package environment.

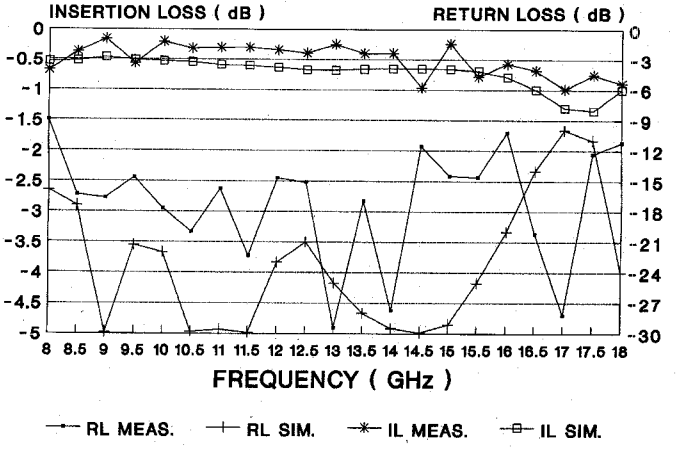

Fig. 4. Measured and predicted insertion loss and return loss of a pair of TWD/C's in a back-to-back configuration.

and effective dielectric constant as a function of the spacing between the package wall and the microstrip line width on a 0.38-mm alumina substrate. Fig. 2 contains a cross-sectional diagram which defines the variables used in this analysis. Table II compares the quasi-microstrip line width required for this design to the microstrip line widths that would have been used for an unpackaged design.

III. Fabrication and Test Results

The TWD/C was fabricated on a 0.38-mm thick alumina substrate. Fig. 3 shows a pair of TWD/C's in a test fixture positioned back to back forming a two port structure. This test fixture was constructed with walls located at the same distance from the microstrip lines as the final packaged TWD/C design. One of the other problems encountered in the fabrication of a miniature TWD/C was the availability of small size isolation resistors. This problem was solved by using ITT's GaAs MMIC process (MSAG) to fabricate $0.25 \times 1.0\,\mathrm{mm}^2$ resistors. These small resistors enable the TWD/C's size to be kept to a minimum and provide minimum parasistics.

The combiners were characterized by measuring S-parameter using TRL de-embedding techniques and Eisenhart connectors. Fig. 4 shows the measured and calculated return loss and insertion loss of a pair of TWD/C's connected back-to-back. The worst case insertion loss is about 1.1 dB across the 8–15-GHz frequency range and less than 0.6 dB across most of the band, which corresponds to a loss of 0.3 dB per combiner. Also, the minimum return loss measured across most of the band was 13 dB.

IV. Conclusion

This TWD/C design enables MMIC based power amplifiers to be realized in very narrow packages and maintains high efficiencies because the losses are kept to a minimum. This design uses custom miniature resistors produced by ITT's standard GaAs MMIC process (MSAG) to reduce the size. Also, this TWD/C incorporates the effects of the package wall into the design by using a full-wave electromagnetic simulator and the test results demonstrate state-of-the-art performance.

References

[1] A. G. Bert and D. Kaminsky, "The traveling-wave divider/combiner," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-28, no. 12, pp. 1468–1473, Dec. 1980.

[2] A. G. Bert, D. Kaminsky, and G. Kantorowicz, "Progress in GaAs FET power combining with the traveling-wave combiner amplifier," *Microwave J.*, vol. 24, no. 7, pp. 69–73, July 1981.

[3] H. Q. Tserng, and P. Saunier, "10–30 GHz monolithic GaAs travel-wave divider/combiner," *Electron. Lett.*, vol. 21, no. 21, pp. 950–951, Oct. 10, 1985.

[4] R. Garg and I. J. Bahl, "Characteristics of coupled microstriplines," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-27, pp. 700–705, July 1979; correction in *IEEE Trans. Microwave Theory Tech.*, vol. MTT-28, p. 272, Mar. 1980.